Technical Note 117

SGS ATES

TDA 1200 FM-IF SYSTEM FOR HIGH PERFORMANCE RADIO RECEIVERS

by
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A detailed description of the equivalent schematic diagram of TDA1200 is given. Then the main electrical characteristics are shown. In addition three application circuits are described with the relative perfomance.

INTRODUCTION

Modern frequency-modulation radio receivers are characterized by auxiliary functions which facilitate their use and improve listening quality.
These auxiliary functions generally require a very complex and costly circuitry, and have therefore in the past been incorporated only in high fidelity equipments.
The integrated circuit TDA1200, by making use of all the advantages provided by the technique of integration, makes it possible to incorporate all these auxiliary functions in a single chip, thus providing a complete high perfomance subsystem at a much lower cost than an equivalent subsystem made up of discrete components.
The functions incorporated in the circuit are:

- amplification, limitation and detection of FM signals at the nominal frequency of 10.7 MHz
- automatic gain and frequency control of the tuner
- automatic muting during tuning and during reception characterized by inadequate signal to noise ratio
- logarithmic indication of the strength of the signal received
- attenuation of side responses of the detector.

The chip size is 71 x 72 mils^2, and the device is packaged in a 16-lead dual in-line plastic case.

DESCRIPTION OF THE CIRCUIT

Block diagram

The block diagram is shown in fig. 1.
The received frequency modulated signal is suitably amplified and converted to a nominal frequency of 10.7 MHz in the tuner, and is then applied, by means of a band-pass filter, to the integrated circuit input (pin 1).
The signal is amplified by a three-stage amplifier-limiter (blocks 1, 2, 3); it is then sent to a parallel limiting circuit (block 4) and to the doubly-balanced coincidence type FM detector (block 5).
The detector produces two low frequency signals 180° out of phase which, suitably combined, provide two outputs, one being the output of the detected audio signal (pin 6), and the other a current output (pin 7) which gives automatic frequency control and indication of tuning precision.
The amplitude of the amplified and limited IF signal is detected by means of four level detectors (blocks 8, 9, 10, 11) during the process described.
The first three detectors (blocks 8, 9, 10) detect the level at the three outputs of the amplifier stages arranged in series; the outputs of the three detectors are added together in block 12 and are available at pin 13, where the amplitude of the signal received can then be monitored.
The three detectors have an intervention threshold which allows them to function only when the relative amplifier stage has reached the limitation threshold point. Clearly, therefore, the first detector (block 8) will be enabled only when the input signal at pin 1 is of a sufficient amplitude to limit the first amplifier stage.
The output of this detector (pin 15) is used then to operate the automatic gain control of the tuner; this control is therefore automatically delayed until the IF signal has reached a sufficient amplitude to be fully limited by all three amplifier stages.
The fourth detector (block 11) measures the signal level at the detector stage input (block 5); or, to be more exact, it measures the signal to noise ratio at this point, and its output (pin 12) is used to provide muting when the signal to noise ratio is inadequate. The muting threshold and the relative signal to noise ratio can be selected externally.
Lastly there is block 13, which is controlled by the detector circuit of the signal to noise ratio (block 11), and serves to switch ON/OFF the detected audio signal output.

ELECTRICAL CHARACTERISTICS OF THE INTEGRATED CIRCUIT (fig. 2)

Below is detailed description of the functional blocks described above.

Amplification and limitation section (blocks 1, 2, 3, 4)

This section comprises three amplifier stages (from Q1 to Q22).
The first amplifier is a differential common-emitter stage (Q1, Q2), which drives a common-base stage (Q3, Q4), thus providing a differential cascode amplifier.
Such a configuration, since it eliminates Miller effect, provides high gain and considerable stability.
The push-pull output of the first stage is sent to the second amplifier (Q10, Q11) by means of two common-collector stages, each of which is Darlington connected (Q8, Q8a and Q7, Q7a respectively).
The outputs of the second stage are sent to the third stage (Q16, Q17) by means of the same system (Q14, Q14a and Q13, Q13a).
The outputs of the third stage, performed by the emitter followers Q19, Q20 and Q21, Q22, are sent back as DC signals to the first amplifier stage inputs, thus producing total negative feedback which gives a very high level of DC stability of the amplifier system.
For AC amplification there is no feedback path, since appropriate bypass capacitors, connected between pins 2, 3 and ground, open the feedback loops.
Two diodes (D2 and D3) are back-to-back connected across the two push-pull outputs of the third stage, and serve to improve the amplitude limitation of the signal.

Detector section (block 5)

The detector section is made up of a doubly balanced multiplier circuit (Q26, Q34; Q24, Q25; Q32, Q33) with two inputs.
The signal from the third amplifier stage,

Fig. 1 - TDA1200 block diagram

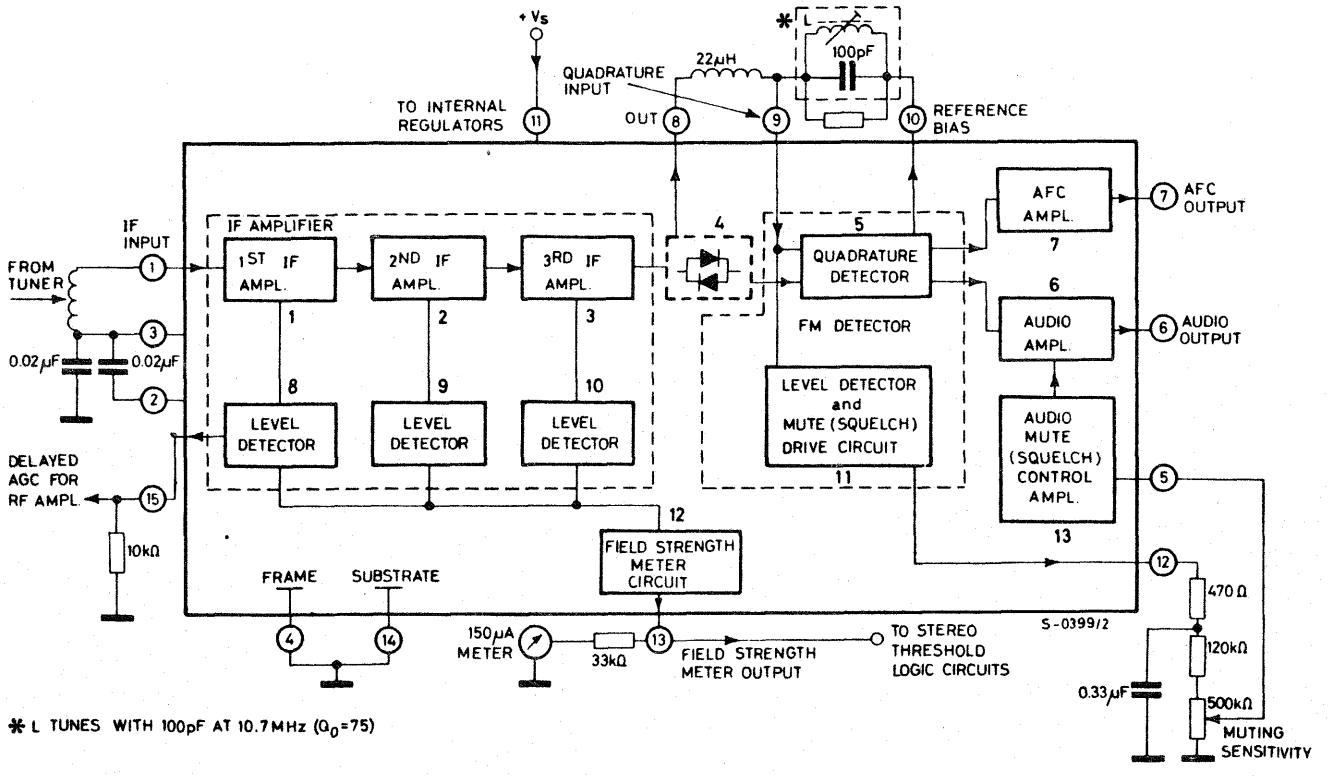
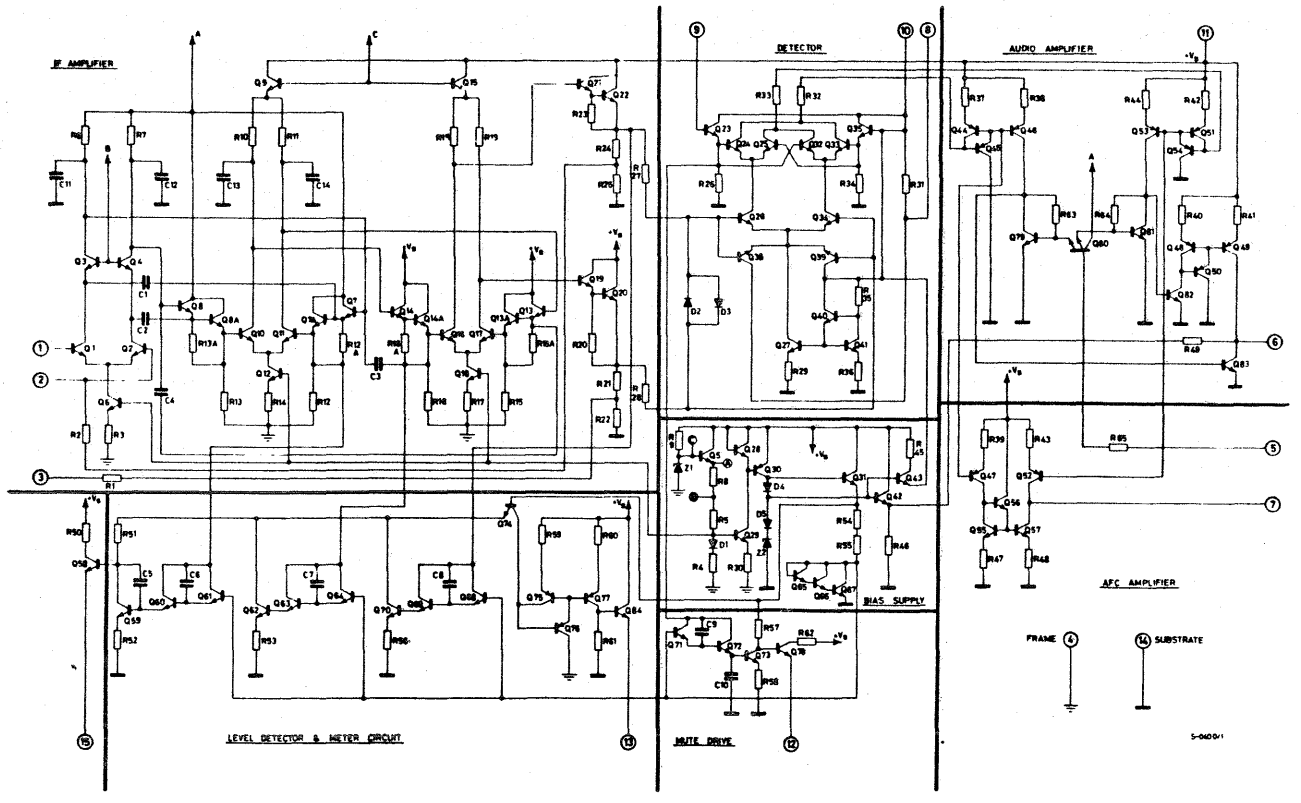


Fig. 2 - TDA1200 schematic diagram



which is limited by two diodes D2 and D3, comes directly to the first input (bases of Q26 and Q34); it reaches the second input (pin 9) by means of an external circuit which introduces a phase-shift proportional to the instantaneous frequency and a static 90° shift at the nominal frequency of 10.7 MHz.
The two transistors (Q38, Q39) constitute a further amplification-limitation differential stage for the signal which feeds the external phase-shift network; the load of this amplifier is made up of the internal resistor R31 and of the phase-shift network connected at pin 8. This limiting stage is situated at this detector input only, in order to improve overall sensitivity without creating problems of stability in the DC feedback loops.
The transistors Q27, Q40 and Q41, constitute the current generator which supplies the multiplier circuit.

Audio output section (block 6), automatic frequency control (block 7), and audio output level control (block 13)

With nominal frequency (10.7 MHz) and perfect balancing of the detector circuit (guaranteed by the high level of symmetry of the chosen configuration), the two currents which flow through resistors R32 and R33 are equal $I_1 = I_2$.
The two currents are sent to two current mirrors made up of Q44, Q45 and Q46 and Q51, Q53 and Q54 respectively.
Two currents proportional to I_1 and I_2 are then available at the collectors of *Q46 and Q53*.
If no voltage is applied at pin 5, the two transistors Q79 and Q81 are OFF, and the two above-mentioned currents flow into the bases of Q83 and Q82 respectively. The Q82 current is then reflected by the current mirror made up of Q48, Q49 and Q50; therefore a current proportional to I_2 flows through the collector of Q49, while a current proportional to I_1 flows through the collector of Q83.
In nominal conditions these two currents are equal: no current flows through R49 and the voltage at pin 6 is the Z2 zener voltage.
When, because of frequency deviation, $I_1 \neq I_2$, the excess current in positive or negative direction which is produced at the collectors of Q49 and Q83 can flow through the internal resistor R49, thus producing the detected audio frequency voltage.
When a suitable voltage is applied at pin 5, the two transistors Q79 and Q81 begin to conduct, so diverting current from the bases of Q83 and Q82, i.e. varying the current which flows at the collectors of Q49 and Q83. In this way it is possible to regulate the amplitude of the voltage detected output.
When Q79 and Q81 conduct all the current supplied by Q46 and Q53 respectively, no current is available at resistor R49 and therefore maximum attenuation of the detected signal is reached (> 60 dB).
AFC circuit (block 7) is operated by an analogous circuit principle.
In this case the two currents I_1 and I_2 are reflected by transistors Q47 and Q52 respectively. The current mirror made up of Q55, Q56 and Q57 transfers current I_1 to the collector of Q57 so that the difference (positive or negative) between the two currents, I_1 and I_2, which flow at the two collectors of Q57 and Q52 can be taken from pin 7.
This difference in current is transferred into voltage variation by connecting a suitable resistor at pin 7.
In this case it was found preferable to use a current output rather than a voltage output, to enable the user to fix the desired value of the slope of the AFC voltage simply by varying the value of the external resistor connected at pin 7.

Level detectors (blocks 8, 9, 10, 11)

There are four signal amplitude *detectors, made up respectively of:* Q59, Q60, Q61; Q62, Q63, Q64; Q70, Q69, Q68; Q71, Q72, Q73, Q78.
The last detector (block 11) Q71, Q72, Q73, Q78 detects the signal after four stages of amplification and limitation, and then operates by means of signals around the input limiting voltage of the device. This detector is used to detect the signal to noise ratio, as will be seen below.
The first three detectors (blocks 8, 9, 10) are identical.
Their respective outputs are added together by means of transistor Q74 and are then sent to output pin 13 by means of a current mirror (Q75, Q76, Q77) (block 12) and an emitter follower Q84, to which the field strength meter may be connected.
Each of the three detectors is biased by

the three diodes Q65, Q66, Q67, and, when no signal is applied, resistors R52, R53, R56 prevent the flow of any current through transistors Q59, Q62, Q70.
When a IF signal of sufficient amplitude is applied at the input of the integrated circuit, this signal is sent by means of a capacitor, e.g. C6, to transistors Q60 and Q61, which act as a voltage doubler detector. The detected signal is amplified by transistor Q59.
The first level detector (block 8), made up of Q59, Q60, Q61, has in addition a supplementary output (pin 15), from which the control signal of the tuner AGC is obtainable.
An emitter follower Q58 is used to increase the current capability.
The fourth level detector (block 11) is not used to supply information regarding signal strength, but serves only to provide muting.
The IF signal present at pin 9 (input of phase-shifted signal) is sent, by means of the emitter follower stage Q23 and capacitor C9, to the junction of the two transistors Q71 and Q72 which, together with capacitor C10, act as detector of the envelope of the signal.
The detected signal is then amplified by Q73 and sent to the output by means of Q78. When the signal at pin 9 has reached the maximum amplitude obtainable at this point, transistor Q73 will be saturated and voltage at pin 12 will be the minimum possible.
When the signal at pin 9 is lower, on the other hand, than this maximum amplitude, the input signal present at pin 1 will be lower than the corresponding value at the limiting threshold, and there will therefore be an inadequate signal to noise ratio. When this is the case, the envelope detector, made up of Q71 and Q72 with C10, produces the so-called "threshold effect", i.e. at certain moments signal and noise cancel each other; no continuous voltage is built up at C10 during these moments and Q73 therefore stops conducting. This effect, which is a nuisance in AM receivers using envelope detection, is in this case put to advantage; the voltage pulses present at the collector of Q73 during these cancellations are rectified by transistor Q78 and by the capacitor connected externally between pin 12 and ground. At this pin a DC voltage is therefore obtained; the amplitude of this voltage is a function of the number of instants in which cancellation between signal and noise occurs, and is therefore also a function of the signal to noise ratio present at the input. This amplitude can therefore be used to provide muting.

Stabilized supply

A stabilized supply circuit contained within the device enables its performance to remain practically unaltered over a fairly wide range of DC voltage applied at pin 11.
The supply voltage regulators are made up of two zener diodes Z1 and Z2 with appropriate thermal compensations and corresponding common-collector current amplifier stages.
The first supplies the amplification-limitation section, while the second supplies the current generator of the frequency modulation detector, the level detectors and the field strength meter; in addition it stabilizes the audio output voltage at pin 6 by means of resistor R49.

TYPICAL PERFORMANCE OF THE CIRCUIT

The circuit's typical perfomance can be measured by means of the test circuit shown in fig. 3.
This circuit has an unbalanced input. Between pins 1 and 3 a resistor of 51Ω is connected.
The phase-shift network is made up of a tuned circuit connected between pins 9 and 10, with a Q factor fixed, by means of a 100 pF capacitor and a parallel connected 3.9 kΩ resistor, at a value representing an appropriate compromise between distortion and amplitude of the detected signal (★).
On completion of the phase-shift network, an inductance is placed between pins 8 and 9, which also serves as a DC path, thus giving correct polarization of the detector, and reduces the content of harmonics present in the phase-shift network, so eliminating likelihood of irradiation, and improving overall stability.
The deemphasis circuit operates by

(★) With these values, and with full limiting, a signal of ~ 150 mV will be available at pin 9. This signal represents a suitable level for the correct functioning of the muting circuit.

means of a 4.7 kΩ resistor which, together with the output impedance of 5 kΩ of pin 6 and the capacitor of 5 nF, gives the required time constant of 50μs. A 4.7 kΩ resistor and a meter with centre dial zero and full scale of ± 100 μA are connected between the AFC output, pin 7, and the stabilized voltage source, pin 10.
The meter acts as a precision tuning indicator.
The potentiometer (470 kΩ), series connected to the 120 kΩ resistor between pin 12 and ground, serves to regulate the point of the muting action. The central tap of the potentiometer is connected to pin 5.
The typical electrical characteristics of the devices obtainable with this test circuit are as follows:

Typical values (V_s = 12V, T_{amb} = 25°C, f_0 = 10.7 MHz)

Supply current	23 mA		
DC voltage (pins 1, 2, 3)	1.9 V		
DC voltage (pin 6)	5.6 V		
DC voltage (pin 7)	5.6 V		
DC voltage (pin 10)	5.6 V		
Input limiting voltage (-3 dB)	12 μV	@	Δf = ±25 kHz
AM rejection	40 dB	@	Δf = ± 25 kHz, m = 0.3 f_m = 1 kHz, V_i > 1 mV
Recovered audio voltage	140 mV	@	Δf = ±25 kHz, f_m = 1 kHz V_i > 50 μV
Total harmonic distortion	0.5 %	@	Δf = ±75 kHz
Capture ratio	1 dB	@	V_i ⩾ 100 μV
Signal and noise to noise ratio	60 dB	@	Δf = ±75 kHz, f_m = 1 kHz V_i ⩾1 mV
Input voltage for delayed AGC action	10 mV		
AGC slope ($\Delta V_{15}/\Delta V_i$)	40 dB	@	V_i ⩾ 10 mV
AFC slope ($\Delta I_7/\delta f$)	1 μA/kHz		
Field strength meter output slope ($\Delta V_{13}/\Delta V_i$)	42 dB		
Field strength meter output sensitivity	1.7 V	@	V_i = 1 mV
Rèduction of audio output signal	55 dB	@	V_5 = 2.4 V

Fig. 3 - TDA1200 test circuit

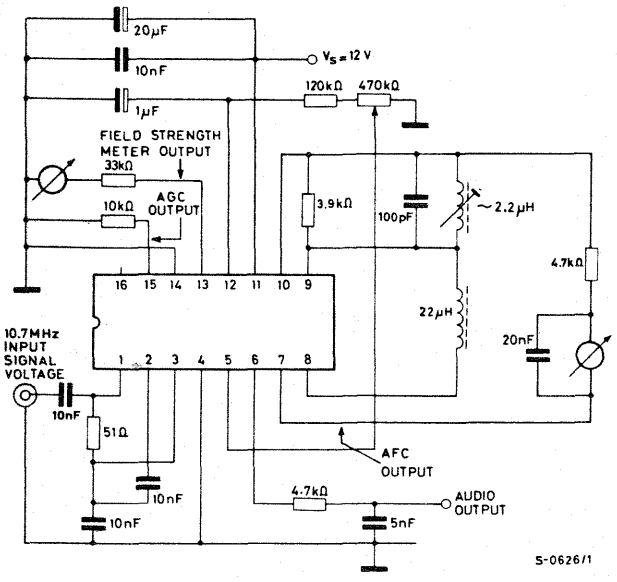


Fig. 4 - Typical relative recovered audio and noise output vs. input voltage

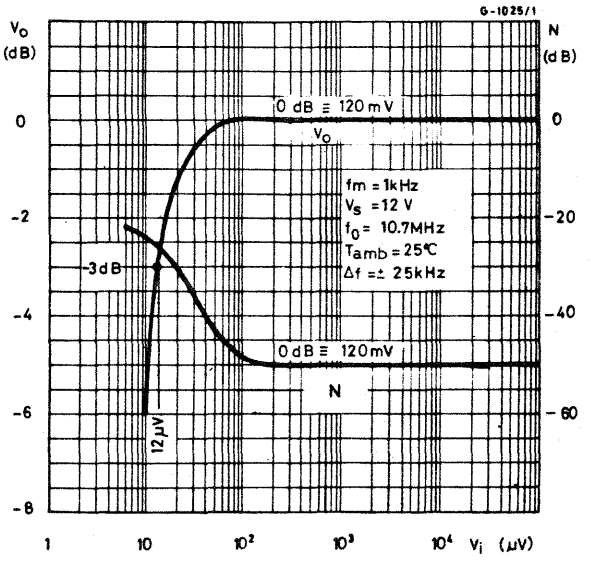


Fig. 5 - Typical capture ratio vs. input voltage

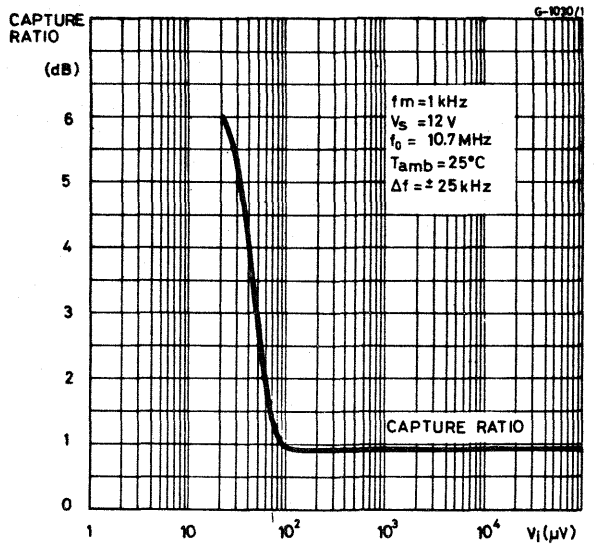


Fig. 6 - Phase-shift network recommended when lower capture ratio and minimum distortion are required

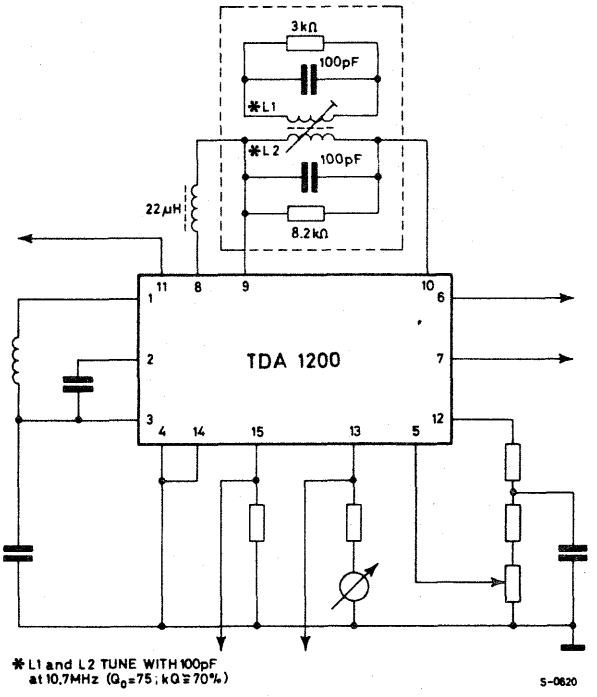


Fig. 4 shows the detected output signal as a function of the input signal.
The circuit can handle fairly high input voltages (> 500 mV) without any deterioration of AM rejection; when functioning normally the AGC of the tuner prevents signals of amplitude greater than 10 mV from reaching the input of the device, since AGC intervention occurs for input signals of approximately 10 mV.
Fig. 4 also shows the detected noise voltage. A signal to noise ratio at the output greater than 20 dB can be obtained, with input voltages in the order of 12 μV.
Fig. 5 shows the capture ratio as a function of the input signal (★). This parameter is measured in the following way: two signals are sent to the test circuit input; the first (V_i at 10.7 MHz) is modulated with a frequency deviation of ±25 kHz and its amplitude is varied as indicated on the abscissa of the diagram in fig. 5.
For each of these values of V_i, the second non-modulated signal (V_i') which has the same nominal frequency of 10.7 MHz, is increased until the audio output of the first signal is reduced by 1 dB. Let this value = V_1'. The non-modulated signal V_i' is therefore further increased to the value of V_2' so that the detected audio output is reduced by 30 dB.
The capture ratio will therefore be:

$$C.R. = 10 \log \frac{V_2'}{V_1'}$$

It should be pointed out that the capture ratio can be decreased to 0.5 dB if the linearity and peak-to-peak separation of the discriminator curve are also increased.
This can be done by means of the phase-shift circuit shown in fig. 6, which also produces a total harmonic distortion of less than 0.1%, even with detuning in the order of ± 100 kHz.
Fig. 7 shows the amplitude modulation rejection. The deterioration which occurs at the limitation threshold zone is due to the wide band noise of the input circuit.
In practical applications, however, the predominat noise is the narrow band noise of the tuning antenna system.
Fig. 8 shows the AM rejection variation as a function of detuning.
This variation is very limited; the performance of the device remains considerably high even without perfect tuning. This may be the case when, for example, the device is used in a car radio, where, among other things, there may be a pulling effect of the tuner oscillator due to adjacent channels.
Fig. 9 shows the typical AGC voltage present at pin 15, and the field strength meter driving voltage (pin 13). The sensitivity of this detection remains practically constant and is equal to approximately 40 dB in the input signal range in which $V_i \leq 10$ mV.
For higher input voltages the linearity is lost, but since in such cases automatic gain control of the tuner intervenes, there is no longer any need to measure the strength of the signal received.
Fig. 10 shows the AFC current at pin 7; the value is positive for currents flowing into pin 7 and negative for currents flowing out of pin 7. This current output is transformed into voltage output by means of a resistor connected between pins 7 and 10.
The value of this resistor may be chosen at will, depending on the frequency-voltage sensitivity of the oscillator present in the tuner. However, it is advisable not to use extremely high resistor values, since a small offset current may be present at pin 7 which could unbalance the central tuning point. This offset current, however, is always less than ± 50 μA.
When the AFC output of the device is not used, it is advisable to link pin 7 to pin 10 with a 4.7 kΩ resistor. This avoids distortion at the audio output which may be caused by feedback at the current translator circuits common to the audio section and the AFC section.

(★) The capture effect is a special feature that takes place in FM receivers. Suppose to have two interferring co-channel signals: if the limiter and the discriminator are capable of accomodating the necessary amplitude and frequency excursions involved, the stronger interferring signal takes over or "captures" the receiver, i.e. the receiver is insensitive to the smaller one. The smaller is the ratio of the two signals amplitude the higher is the quality of the FM receiver.

Fig. 7 - Typical amplitude modulation rejection vs. input voltage

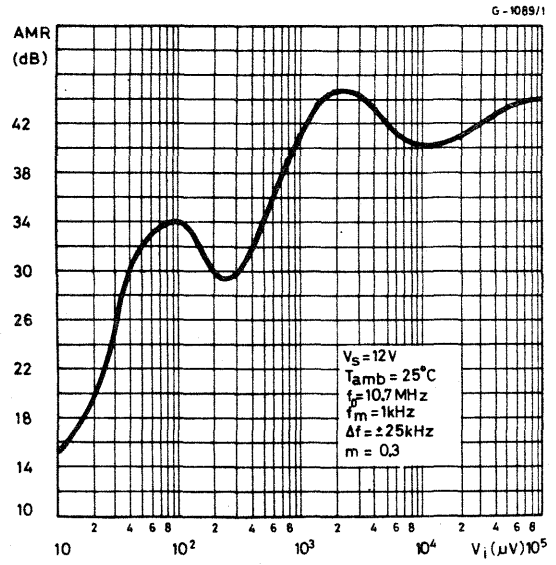


Fig. 8 - Typical AMR vs. change-in tuning frequency

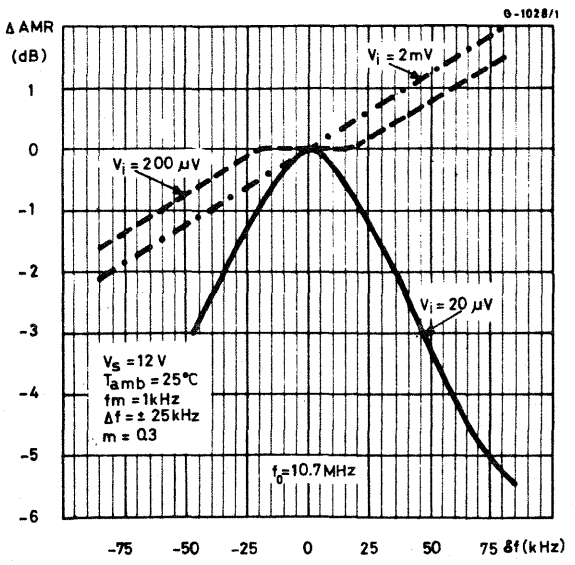


Fig. 9 - Typical AGC (V_{15}) and field strength meter output (V_{13}) vs. input voltage

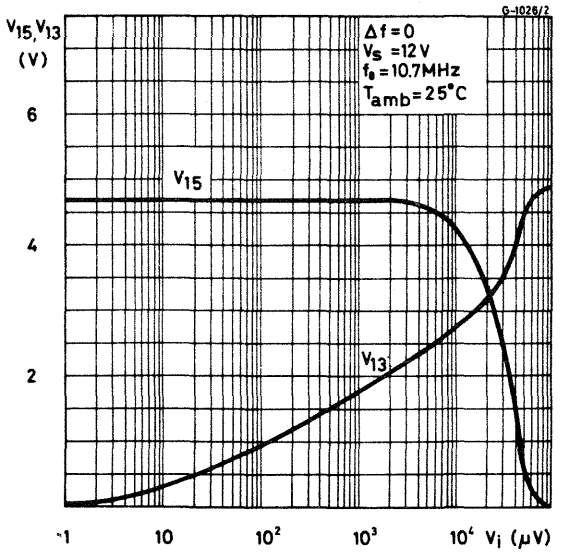
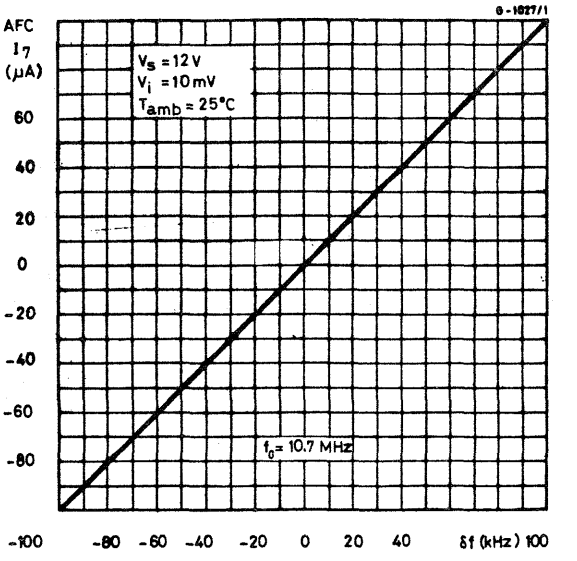


Fig. 10 - Typical AFC output current vs. change-in tuning frequency



APPLICATIONS OF THE TDA1200

By way of example, here are some typical applications of the TDA1200, complete with useful notes for putting them into practice. The most important perfomance figures are also quoted.

High perfomance FM tuner

Fig.11 shows a typical circuit realization of an FM tuner of "Hi-Fi" quality. The tuner is supplied from 15V and covers the 87 to 105 MHz band. Typical values of the most important perfomance parameters are shown in the table below. If a varicap tuner is employed, the AFC circuit of fig.12 can be used (with a control voltage from 1 to 16V).

AM/FM car radio

The circuit diagram of the car radio is shown in fig. 13.
The receiver, which is typically, supplied at 14.4V uses 3 integrated circuits which perform the following functions:

TDA1200 FM-IF (10.7 MHz) subsystem and auxiliary circuits

TBA651 RF amplifier for AM, convertor with separate oscillator, AM-IF amplifier, AGC circuit

TBA810S complete audio amplifier.

The only discrete components are those of the FM tuner. The receiver uses 2 ceramic filters for good FM selectivity. The main perfomance parameters are given in the table below.

Portable AM/FM radio

Fig.14 shows the circuit diagram of a good quality AM/FM receiver using the TDA1200, TBA651 and TCA830 integrated circuits. It may be supplied from the mains or a 9V battery.
It uses ceramic filters.
The performance of this receiver is also shown below.

Typical perfomance (T_{amb} = 25°C, f_m = 1 kHz, $\frac{S+N}{N}$ = 20 dB, unless otherwise specified)

HIGH PERFORMANCE FM TUNER		
Input limiting voltage	$V_i \leq 1.2\ \mu V$	@ f_0 = 87 to 105 MHz
Input signal level	$V_i \leq 0.7\ \mu V$	@ $\Delta f = \pm 75$ kHz, $R_g = 50\ \Omega$
AM/FM CAR RADIO		
AM input signal level (pin 1 of TBA651)	$V_i \leq 10\ \mu V$	@ f_0 = 1 MHz, m = 0.3
FM input signal level (antenna)	$V_i \leq 1\ \mu V$	@ f_0 = 98 MHz, $\Delta f = \pm 75$ kHz, $R_g = 50\ \Omega$
Audio output power	$P_o = 6$ W	@ d = 10 %, $R_L = 4\ \Omega$
PORTABLE AM/FM RADIO		
AM input signal level (pin 1 of TBA651)	$V_i \leq 10\ \mu V$	@ f_0 = 1 MHz, m = 0.3
FM input signal level (antenna)	$V_i \leq 2\ \mu V$	@ f_0 = 98 MHz, $\Delta f = \pm 75$ kHz, $R_g = 50\ \Omega$
Audio output power	$P_o = 2$ W	@ d = 10 %, $R_L = 4\ \Omega$

Fig. 11 - Circuit diagram of high perfomance FM tuner

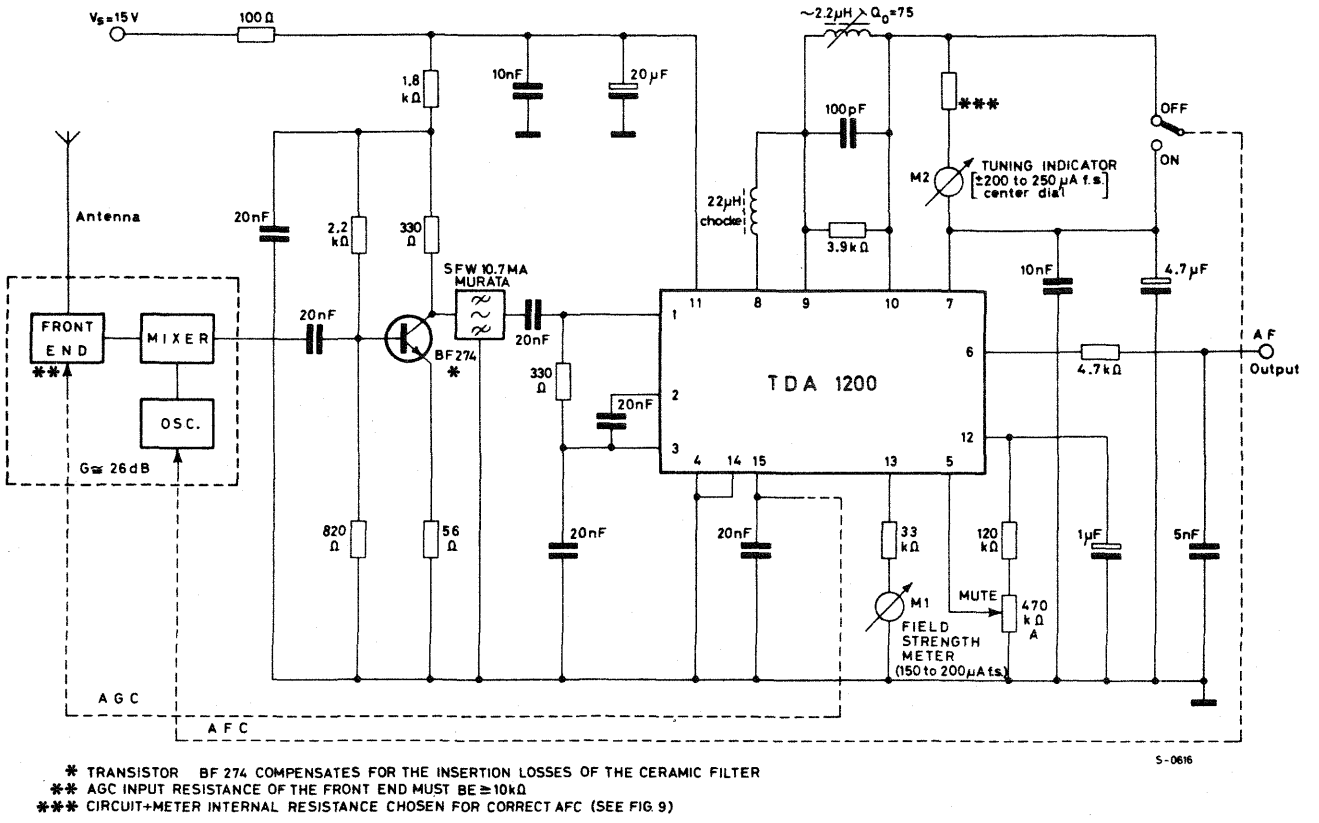


Fig. 12 - AFC circuit and DC control for varicap tuner

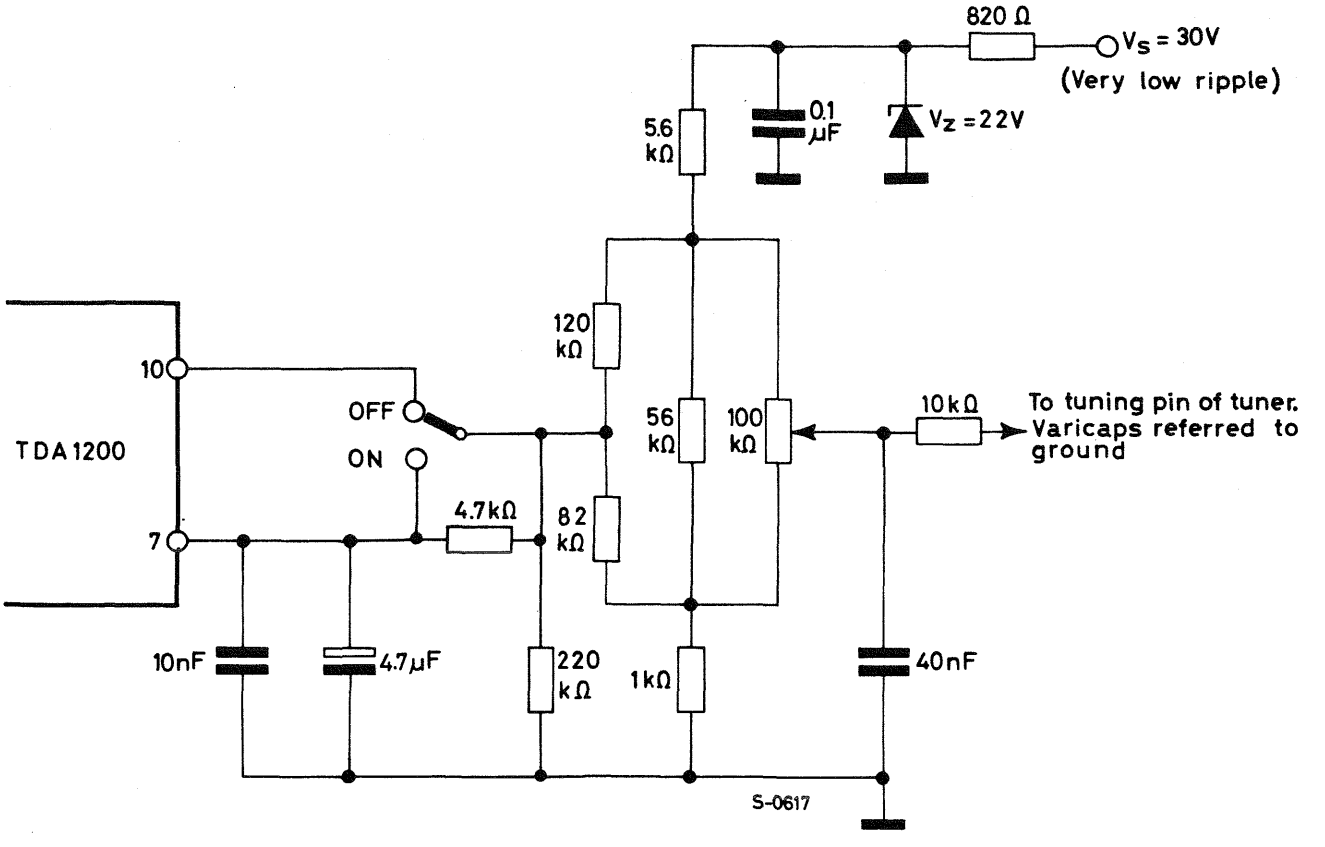


Fig. 13 - AM/FM car radio circuit diagram

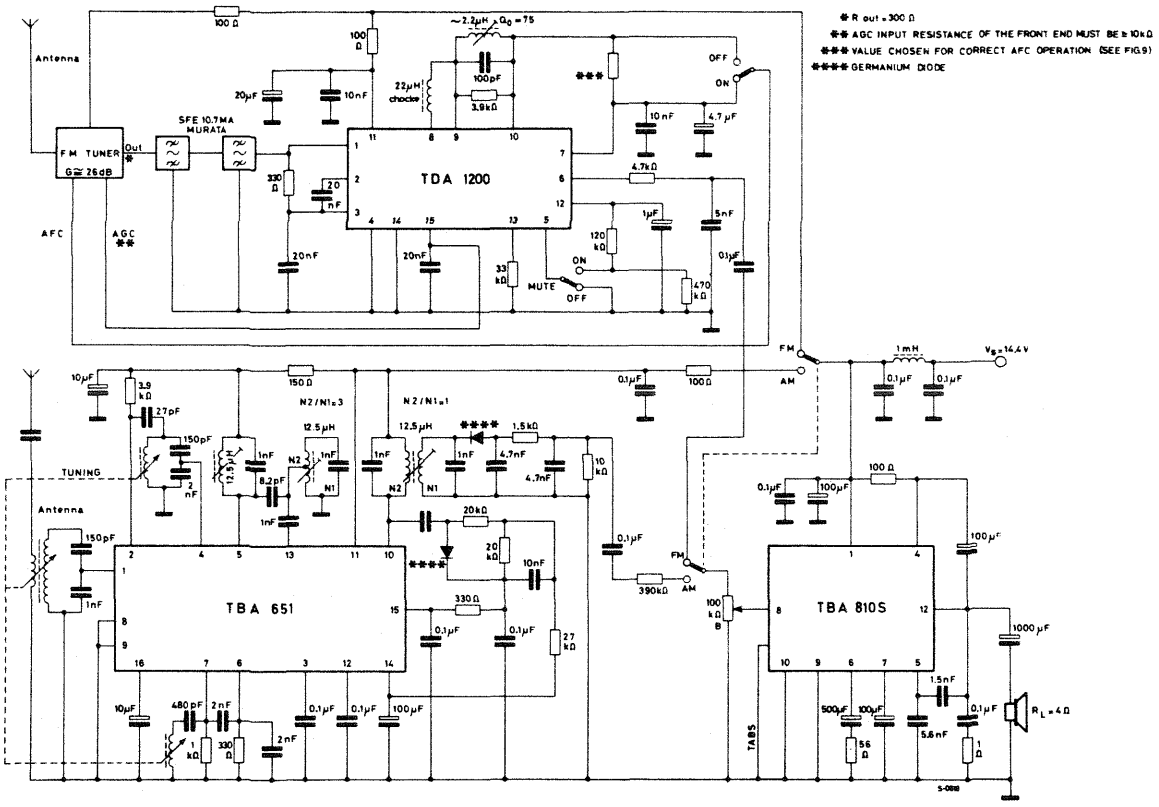


Fig. 14 - Circuit diagram of AM/FM portable radio